| Class | Subclass | ISSUE CLASSIFICATION |
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PATENT NUMBER

# U.S. UTILITY Patent Application

| O.I.P.E. | PATENT DATE |
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| APPLICATION NO. | CONT/PRIOR | CLASS | SUBCLASS | ART UNIT | EXAMINER |
|---|---|---|---|---|---|
| 09/663021 | D | 257 | 750 | ~~2811~~ 2815 | E. Clark |

APPLICANTS: Kai Young

TITLE: Self-aligned semiconductor interconnect barrier and manufacturing method therefor

PTO-2040 12/89

| Drawing | Fig. Drawing | Print Fig. | |
|---|---|---|---|
| | | | |

(Assistant Examiner) (Date)

(Primary Examiner) (Date)

(Legal Instruments Examiner) (Date)

NOTICE OF ALLOWANCE MAILED

ISSUE FEE

Amount Due | Date Paid

ISSUE BATCH NUMBER

☐ The terminal ____ months of this patent have been disclaimed.

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